



Attorney Docket No.: YOR920030258US1

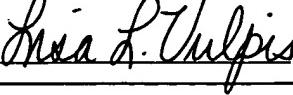
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): W. Rhee et al.
Docket No.: YOR920030258US1
Serial No.: 10/697,751
Filing Date: October 30, 2003
Group: To Be Assigned
Examiner: To Be Assigned

Title: Voltage-Controlled Delay Circuit Using
Second-Order Phase Interpolation

I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class mail addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Signature:  Date: January 30, 2004

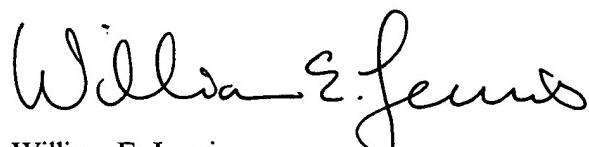
TRANSMITTAL OF FORMAL DRAWINGS

Mail Stop PGPUB Drawings
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants submit herewith five (5) sheets of formal drawings in the above-referenced patent application.

Respectfully submitted,



William E. Lewis
Reg. No. 39,274
Attorney for Applicant(s)
Ryan, Mason & Lewis, LLP
90 Forest Avenue
Locust Valley, NY 11560
(516) 759-2946

Date: January 30, 2004